Main Conference Program: Day 1 (January 5, 2015)				
Registration: 7.30 AM to 9.00 AM				
Inauguration: 9.00 AM to 9.40 AM				
Vision Talk 1: 9.45 AM to 10.30 AM				
Tea/Coffee Break: 10.30 AM to 10.45 AM				
Vision Talk 2: 10.45 AM to 11.30 AM				
Panel Discussion: 11.35 AM to 12.15 PM				
Key Note 1: 12.20 AM to 1.00 PM				
Lunch, Day 1:1.00 PM to 2.00 PM				
Key Note 2: 2.00 PM to 2.40 PM				
Track A	**Track B**	**Track C**	**Track D**	**Track E**
Session1, Day 1:2.45 PM to 3.45 PM				
Session A1: Embedded Systems	**Session B1: Design Verification**	**Session C1: Analog**	**Session D1: Industry Forum**	**Session E1: User Design**
A1.1 ARGUS: A Framework for Rapid Design and Prototype of Heterogeneous Multicore Systems in FPGA - Jude Angelo Ambrose, Tuo Li, Daniel Murphy, Shivam Gargg, Nick Higgins and Sri Parameswaran	B1.1 On-The-Fly Donut Formation in Compiled Memory - Darvinder singh, Isha Garg, Vineet Sachan and Prasanna Nalawar	C1.1 On Slew Rate Enhancement in Class-A Opamps Using Local Common-Mode Feedback - Rakshitdatta K. S and Nagendra Krishnapura		
A1.2 Parameterizable FPGA framework for particle filter based object tracking in video - Pinalkumar Engineer, Velmurugan Rajbabu and Sachin Patkar	B1.2 Scaling the uvm_reg model towards automation and simplicity of use - Abhishek Jain, Dr. Hima Gupta, Jose Mangione and Dr. Fabrice Baray	C1.2 Accurate Constant Transconductance Generation Without Off-chip Components - Imon Mondal and Nagendra Krishnapura		
A1.3 RELSPEC: A Framework for Early Reliability Refinement of Embedded Applications - Saurav Kumar Ghosh, Aritra Hazra and Soumyajit Dey	B1.3 On the Analysis of Reversible Booth's Multiplier - Sajib Mitra, Ahsan Chowdhury and Jakia Sultana	C1.3 Ultra-fast cap-less LDO for dual lane USB in 28FDSOI - Saurabh Singh and Gautam Kanungo		
Tea/Coffee Break: 3.45 PM to 4.00 PM				

Track A	Track B	Track C	Track D	Track E
Session 2, Day 1:4.00 PM to 5.30 PM				
Session A2: Embedded Systems	**Session B2: Design Implementation**	**Session C2: Analog**	**Session D2: Industry Forum**	**Session E2: User Design**
A2.1 Thermal Extension of the Total Bandwidth Server – Ayoosh Bansal, Rehan Ahmed, Bhuvana Kakunoori, Parameswaran Ramanathan and Kewal Saluja	B2.1 Invited Talk: Better-than-Worst-Case Timing Design – Adit Singh, Auburn University, USA	C2.1 Invited Talk: RF/Analog design challenges in Advanced Technology Nodes – Madhukar Reddy, V.P. Central Engineering, Maxlinear Inc., USA		
A2.2 Thermal-Aware Test Data Compression Using Dictionary Based Coding – Rajit Karmakar and Santanu Chattopadhyay	B2.2 Two Phase Write Scheme to Improve Low Voltage Write-Ability in Medium-Density SRAMs – M Sultan M Siddiqui, Shailendra Sharad, Yogendra Sharma and Amit Khanuja	C2.2 Any Capacitor Stable LVR Using Sub-Unity Gain Positive Feedback Loop in 65nm CMOS – Saurabh singh and Nitin Bansal		
A2.3 CERI: Cost-Effective Routing Implementation Technique For Network-on-Chip – Rimpy Bishnoi, Vijay Laxmi, Manoj Singh Gaur, Radi Husin Bin Ramlee and Mark Zwolinski	B2.3 A CMOS 90nm Supply Noise Tolerant High Density 8T –NAND ROM – Vinay Kumar, Ashish Kumar and Dhori Kedar Janardan	C2.3 A Wide Dynamic-Range Low-Power Signal Conditioning Circuit for Low-Side Current Sensing Application – Rahul T., Bibhudatta Sahoo, Arya Sasidharakurup, Parvathy S. J. and Veeresh Babu Vulligaddala		
A2.4 Way Halted Prediction Cache: An Energy Efficient Cache Architecture for Embedded Processors – Neethu Mallya, Geeta Patil and Biju Raveendran	B2.4 2SAT based Infeasibility Resolution during Design Rule Correction on Layouts with Multiple Grids – Sambuddha Bhattacharya , Nitin Salodkar, Subramanian Rajagopalan, and Shabbir Batterywala	C2.4 A wide tuning range LC quadrature phase oscillator employing mode switching – Sivaramakrishna Rudrapati, Sharayu Jagtap and Shalabh Gupta		
Fire Side Chat : 5.30 PM to 6.00 PM				
BOF: Topic TBD: 6.00 PM to 7.00 PM				

Main Conference Program: Day 2 (January 6, 2015)				
Registration: 7.30 AM to 9.00 AM				
Vision Talk 3: 9.00 AM to 9.45 AM				
Panel Discussion: 9.50 AM to 10.50 AM				
Tea/Coffee Break: 10.50 AM to 11.05 AM				
Vision Talk 4: 11.10 AM to 11.55 AM				
Track A	**Track B**	**Track C**	**Track D**	**Track E**
Session 1, Day 2: 12.00 PM to 1.00 PM				
Session A3: Special Session	**Session B3: Design Verification**	**Session C3: Devices & Circuits**	**Session D3: Industry Forum**	**Session E3: User Design**
A3.1 Special Session : IoT Protocol Wars & the Way Forward - Virendra Gupta and Jayaraghavendran, Huawei Technologies, India	B3.1 Formal Methods for Pattern Based Reliability Analysis in Embedded Systems - Sumana Ghosh and Pallab Dasgupta	C3.1 Block-level Electro-Migration Analysis(BEMA)for safer product life - Radhika Gupta, Rakesh Shenoy Panemangalore and Atul Bhargava		
A3.2 Invited Talk: Environmental Pollution Monitoring : Gas Sensors to System Integration - Navkant Bhatt, Indian Institute of Science	B3.2 On Event Driven Modeling of Continuous Time Systems - Dushyant Juneja	C3.2 Recessed MOSFET in 28 nm FDSOI for better breakdown characteristics - Kranthi Nagothu, RadhaKrishnan Sithanandam and Rama S. Komaragiri		
		C3.3 A noise aware CML latch modelling for large system simulation - Abhijit Chatterjee, Debesh Bhatta and Suvadeep Banerjee		
Lunch, Day 2:1.00 PM to 2.00 PM				
Key Note 3: 2.00 PM to 2.40 PM				

Track A	Track B	Track C	Track D	Track E
Session 2, Day 2: 2.45 PM to 3.45 PM				
Session A4: IOT & Product	**Session B4: Design Implementation**	**Session C4: Devices & Circuits**	**Session D4: Test & Reliability**	**Session E4: User Design**
A4.1 A Frequency Scan Scheme for PLL-Based Locking To High-Q MEMS Resonators - Anjan Kumar, Abhinav Dikshit, Bill Clark and Jeff Yan	B4.1 A Novel CKE-ODT-CSN Encoding Scheme in DDR Memory Interface - Vinod Inipodu Murugan, Sendhil Arul and Narayanan Mayandi	C4.1 Design of high speed ternary full adder and three-input XOR circuits using CNTFETs - Anu Gupta and Snehlata Murotiya	D4.1 New Methods for Simulation Speed-up and Test Qualification With Analog Fault Simulation - Lakshmanan Balasubramanian, Devanathan VR and Rubin Parekhji	
A4.2 NFC Products For Pervasive Healthcare - Prabhakar T V, Ujwal Mysore, Uday Singh Saini, Vinoy K J and Bharadwaj Amruthur	B4.2 A Design Approach for Compressor Based Approximate Multipliers - Naman Maheshwari, Zhixi Yang, Jie Han and Fabrizio Lombardi	C4.2 An Efficient Transition Detector Exploiting Charge Sharing - Yu Wang and Adit Singh	D4.2 Efficient Peak Power Estimation using Probabilistic Cost-Benefit Analysis - Prabhat Mishra, Hadi Hajimiri and Kamran Rahmani	
A4.3 Hardware Solution For Real-time Face Recognition - Gopinath Mahale, Hamsika Mahale, Arnav Goel, S.K. Nandy, Sukumar Bhattacharya and Ranjani Narayan	B4.3 Integrated 16-channel Transmit and Receive Beamforming ASIC for Ultrasound Imaging - Chandrashekar Dusa, Samiyuktha Kalalii, Omkeshwar B and Rajalakshmi P	C4.3 A High-Efficiency Switched-Capacitance HTFET Charge Pump For Low-Input-Voltage Applications - Xueqing Li, Unsuk Heo, Huichu Liu, Sumeet Gupta, Suman Datta and Vijaykrishnan Narayanan	D4.3 DFT Technique for Quick Characterization of Flash Offset in Pipeline ADCs - Pradeep Nair and Nagarajan Viswanathan	
Tea/Coffee Break: 3.45 PM to 4.00 PM				
Track A	**Track B**	**Track C**	**Track D**	**Track E**
Session 3, Day 2: 4.00 PM to 5.30 PM				
Session A5: Product & Emerging Technologies	**Session B5: Design Implementation**	**Session C5: Special Session on Sensors**	**Session D5: Test & Reliability**	**Session E5: User Design**
A5.1 Invited Talk: Challenges in Nanodevice Technology - Murali Kota, Distinguished Member Technical Staff, Global Foundries	B5.1 Thermal-aware application scheduling on device-heterogeneous embedded architectures - Karthik Swaminathan, Jagadish Kotra, Huichu Liu, Jack Sampson, Mahmut Kandemir and Vijaykrishnan Narayanan	C5.1: Invited Session 1: Sensors to Systems to Applications - Ramgopal Rao, IIT Mumbai	D5.1 Invited Talk: Recent Advances in Test Compression - Nilanjan Mukherjee, Engineering Director, Test Synthesis, Silicon Test Solution, Mentor Graphics Corp., USA	

A5.2 Towards a Real-Time Smart Water Monitoring System - Vignesh Kudva, Prashanth Nayak, Bharadwaj Amrutur, Mohan Kumar, Anjana G.R, Alok Rawat and Sheetal Kumar	B5.2 Exploring Scope of Power Reduction with Constrained Physical Synthesis - Kaustav Guha, Sourav Saha and Ricardo Nigaglioni		D5.2 Framework for Selective Flip-Flop Replacement for Soft-Error Mitigation - Pavan Vithal Torvi, Devanathan VR and Kamakoti V
A5.3 Robot navigation using neuro-electronic hybrid systems - Jude Baby, Grace Mathew Abraham, Bharadwaj Amrutur and Sujit Kumar Sikdar	B5.3 All Optical Implementation of Mach-Zehnder Interferometer based Reversible Sequential Counters - Pratik Dutta, Chandan Bandyopadhyay and Hafizur Rahaman	C5.2: Invited Session 2: Development of MEMS sensors for agriculture - R. P. Singh	D5.3 Diagnostic Tests for Pre-Bond TSV Defects - Bei Zhang and Vishwani Agrawal
A5.4 Comparison of Off-chip Training Methods for Neuromemristive Systems - Cory Merkel and Dhireesha Kudithipudi	B5.4 Design of a Compact Reversible Carry Look-Ahead Adder Using Dynamic Programming - Nusrat Jahan Lisa and Hafiz Md Hasan Babu		D5.4 Few Good Frequencies for Power-Constrained Test - Sindhu Gunasekar and Vishwani Agrawal
Panel Discussion : 5.35 PM to 6.15 PM			
Ideathon Display: 6.20 PM to 7.00 PM			
Banquet Address: 7.05 PM to 7.45 PM			
Awards Ceremony and Others: 7.45 PM to 9.00 PM			
Banquet Dinner: 9.00 PM to 10.30 PM			

Main Conference Program: Day 3 (January 7, 2015)				
Registration: 7.30 AM to 9.00 AM				
Vision Talk 5: 9.00 AM to 9.45 AM				
Panel Discussion: 9.50 AM to 10.50 AM				
Tea/Coffee Break: 10.50 AM to 11.05 AM				
Vision Talk 6: 11.10 AM to 11.55 AM				
Track A	**Track B**	**Track C**	**Track D**	**Track E**
Session 1, Day 3: 12.00 PM to 1.00 PM				
Session A6: System Level Design	**Session B6: Panel Discussion**	**Session C6: Digital & FPGA**	**Session D6:Test & Reliability**	**Session E6: User Design**
A6.1 OcNoC: Efficient One-cycle Implementation of Routers for 3D Mesh Networks on Chip - Lucas Brahm, Ramon Fernandes, Thais Webber, Rodrigo Cataldo, Letícia B. Poehls and César Marcon	B6.1: Global Technology Progress in VLSI and Embedded Systems	C6.1 Power Optimization Techniques for DDR3 SDRAM - Preeti Ranjan Panda, Vishal Patel, Praxal Shah, Namita Sharma, Vaidyanathan Srinivasan and Dipankar Sarma	D6.1 Invited Talk: Volume Diagnosis for Yield Improvement - Wu-Tung Cheng, Mentor Graphics Corp., USA and Sudhakar M. Reddy, University of Iowa, USA	
A6.2 Mode-Division-Multiplexed Photonic Router for High Performance Network-on-Chip - Dharanidhar Dang, Biplab Patra, Rabi Mahapatra and Martin Fiers		C6.2 A Novel Ternary Content-Addressable Memory (TCAM) Design Using Reversible Logic - Dinesh Kumar Selvakumaran and Noor Mahammad Sk	D6.2 Using Boolean Tests to Improve Detection of Transistor Stuck-open Faults in CMOS Digital Logic Circuits - Xijiang lin, Sudhakar Reddy and Janusz Rajski	
A6.3 A Hardware and Thermal Analysis of DVFS in a Multi-Core System with Hybrid WNoC Architecture - Sri Harsha Gade, Hemanta Kumar Mondal and Sujay Deb		C6.3 Design and Analysis of Delay Elements for 2-Phase Bundled-Data Asynchronous Circuits - Guilherme Heck, Leandro Sehnem Heck, Ajay Singhvi, Matheus Trevisan Moreira, Peter Beerel and Ney Laert Vilar Calazans	D6.3 On-Chip Current Sensors and Neighbourhood Comparison Logic to Detect Resistive-Open Defects in SRAMs - Felipe Lavratti, Leticia Maria Bolzani Poehls, Fabian Luis Vargas, Andrea Calimera and Enrico Macii	
Lunch, Day 2:1.00 PM to 2.00 PM				
Key Note 4: 2.00 PM to 2.40 PM				

Track A	Track B	Track C	Track D	Track E
Session 2, Day 3: 2.45 PM to 3.45 PM				
Session A7:System Level Design	**Session B7: TBD**	**Session C7: Digital & FPGA**	**Session D7: EDA**	**Session E7:User Design**
		C7.1 FPGA Implementation of an Advanced Encoding and Decoding Architecture of Polar Codes - mamatha oommen	D7.1 Statistical Analysis of 64Mb SRAM for Optimizing Yield and Write Performance - Gaurav Narang, Pragya Sharma, Mansi Jain and Anuj Grover	
A7.1 Bandwidth Adaptive Nanophotonic Crossbars with Clockwise/Counter-Clockwise Optical Routing - Matthew Kennedy and Avinash Kodi		C7.2 Low-Area and Low-Power Reconfigurable Architecture for Convolution-Based 1-D DWT using 9/7 and 5/3 Filters - Basant Mohanty, Pramod Meher and M.N.S Swamy	D7.2 Recursive Wirelength Model for Analytical Placement - BNB RAY and Shankar Balachandran	
A7.2 Effects of Nondeterminism in Hardware and Software Simulation with Thread Mapping - Giordano Salvador, Siddharth Nilakantan, Ankit More, Baris Taskin and Mark Hempstead		C7.3 SPAA-Aware 2D Gaussian Smoothing Filter Design Using Efficient Approximation Techniques - Ankur Jaiswal, Bharat Garg, Vikas Kaushal and G K Sharma	D7.3 A Nonlinear Analytical Optimization Method for Standard Cell Placement of VLSI Circuits - Sameer Pawanekar, Kalpesh Kapoor and Gaurav Trivedi	
Tea/Coffee Break: 3.45 PM to 4.00 PM				
Track A	**Track B**	**Track C**	**Track D**	**Track E**
Session 3, Day 3: 4.00 PM to 5.30 PM				
Session A8: HPC	**Session B8: LOC**	**Session C8: Digital & FPGA**	**Session D8: EDA**	**Session E8: User Design**
A8.1 Can you trust your memory trace?: A comparison of memory traces from binary instrumentation and simulation - Siddharth Nilakantan, Scott Lerner, Mark Hempstead and Baris Taskin	B8.1 Special Session : Continuous-Flow Biochips: Current platforms and emerging research challenges - Paul Pop, Technical University of Denmark (DTU), Denmark	C8.1 An FPGA-based Architecture for Local Similarity Measure for Image/Video Processing Applications - Jai Gopal Pandey, Abhijit Karmakar, Chandra Shekhar and S. Gurunarayanan	D8.1 Monitoring AMS Simulation: From Assertions to Features - Antara Ain and Pallab Dasgupta	

A8.2 Exploration of Migration and Replacement Policies for Dynamic NUCA over Tiled CMPs - Shirshendu Das and Hemangee K. Kapoor	C8.2 FPGA based Scalable Fixed Point QRD core using Dynamic Partial Reconfiguration - Gayathri R Prabhu, Bibin Johnson and Dr. J Sheeba Rani	D8.2 BDD-based Synthesis for All-optical Mach-Zehnder Interferometer Circuits - Eleonora Schonborn, Kamalika Datta, Robert Wille, Indranil Sengupta, Hafizur Rahaman and Rolf Drechsler
A8.3 Cross-Layer Exploration of Heterogeneous Multicore Processor Configurations - Santanu Sarma and Nikil Dutt	C8.3 A High-performance Energy-efficient Hybrid Redundant MAC for Error-resilient Applications - Sunil Dutt, Anshu Chauhan, Rahul Bhadoriya, Sukumar Nandi and Gaurav Trivedi	D8.3 Optimized Logarithmic Barrel Shifter in Reversible Logic Synthesis - Sajib Mitra and Ahsan Chowdhury
A8.4 Micro-architectural Enhancements in Distributed Memory CGRAs for LU and QR Factorizations - Farhad Merchant, Arka Maity, Mahesh Mahadurkar, Kapil Vatwani, Ishan Munje, Madhava Krishna, Nalesh S, Nandhini Gopalan, Soumyendu Raha, S K Nandy and Ranjani Narayan	C8.4 Energy Aware Computation Driven Approximate DCT Architecture for Image Processing - Vikas Kaushal, Ankur Jaiswal, Bharat Garg and G. K. Sharma	
VC Start-Up Session : 5.35 PM to 6.30 PM		